RESEARCH ARTICLE OPEN ACCESS

Hardware Solution to Motion Object Detection Using Morphological Filtering and FPGA

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Abstract
Moving Object detection applications popularly uses background subtraction method where the stable background image is subtracted from each frame to detect the moving object. Most of these applications are software based applications which are relatively slower and inaccurate. This paper presents an innovative and unique hardware solution using morphological filtering technique and we observe a output on visual basic hyperlink terminal. This solution is based on Microblaze architecture of Spartan 3 EDK FPGA. Field Programmable Gate Arrays (FPGA) are commonly used for implementing complex image processing algorithm applications.
Index terms: FPGA, Background subtraction, Morphological filter, dilation, erosion, Image processing

I. INTRODUCTION

As mentioned in abstract, currently Image Processing applications are widely implemented by using software (mostly MATLAB) which are not very accurate. This paper presents innovative background subtraction algorithm which is realized using Spartan 3 FPGA consisting of Microblaze processor to increase the execution speed. It also consists of high no of MAC units than the DSP processors to further accelerate the operations in the FPGA. The main objective behind this concept is to obtain more accurate results using with high speed using hardware solution. We are using FPGA to implement hardware in the existing Image Processing applications. Field Programmable Gate Arrays (FPGA) are widely implemented as reconfigurable devices those can be used in an area of Image Processing [7][9]. FPGA consists of abundant digital components like look up tables, logic gates, flip-flops and many more along with memory. Numerous innovative designs can be implemented by reconfiguring the logic in an FPGA.

In proposed approach, an extremely configurable Microblaze processor is used, an algorithm is written in system C coding and synthesized using the XILLINX Platform Studio 10.1 and the output are observed through Visual Basis based application which extracts the pixel values of an image that comes from the FPGA to computer through UART communication.

Also as mentioned in abstract, background subtraction is a popular image processing technique used in the video surveillance applications in which an image's foreground is extracted for additional processes like object recognition. Typically such applications are interested to extract moving objects like humans, cars etc. from the image. Mostly this information is extracted by subtracting the stable background image from each frame of static camera videos [1].

Background subtraction is used as a category of techniques for segmenting out objects of interest in very useful applications like police investigation. There are certain challenges in developing an ideal background subtraction algorithmic rule. Primary challenge is to keep it strong against changes in brightness level. Second challenge is to avoid detection of dynamic background objects like shadows by moving objects. An ideal background model should react quickly to changes in background and adjust itself to accommodate changes occurring within the background like moving of a stationary chair from one place to a different. It should also have a decent foreground detection rate and the constant time interval for background subtraction.

II. THE PROPSED APPROACH

The revised approach in this paper has three main phases as below [12]:
a. Background subtraction
b. Using morphological filter to remove noise and
c. Implement a linear filer technique

Background subtraction is a common method to detect moving objects by constantly capturing current image and comparing it with static background image. The success of this method lies in the initialization and updation of background image and detection of accurate moving objects. This background reference image needs to be updated in

some cases for example when a chair is moved or added from background.

The major goal of image enhancement is to improve the visibility and perceptibility of several regions and also the detectability of the image features in these regions. This goal can be achieved through various tasks such as: cleaning various types of noises from an image; enhancing the contrast among neighboring regions; simplifying the image by selective smoothing or removing and retaining the features at various scales. Traditional approaches mainly uses linear system tools to achieve these goals, however it is commonly observed that such linear approaches are not suitable to solve problems related to geometrical aspects of an image. This gives birth to the need for nonlinear approaches. Mathematical morphology is one of such a powerful nonlinear methodology that can successfully solve the said problems [14].

Morphology is an image processing solution which compares each pixel in an image with its neighboring pixels and then reassigns the value based on specific operation.

The main two operations in the morphology are

A. Dilation
B. Erosion

Both these operations requires an input image to process and the structured element which is nothing but a set of coordinates or pattern as shown in fig 2.1 below

4 neighbors 8 neighbors

Figure 2.1 Structuring elements for morphological operations

In first structuring element, each pixel value is compared with only vertical and horizontal neighbor pixels whereas in second structuring element the pixel value is compared with vertical, horizontal and diagonal neighbor pixels.

Erosion:

Erosion removes the pixels at the boundaries of an image.

In Erosion operation, the neighboring pixels are identified for each pixel in input image. These neighbors are identified as per the structuring element. Then the minimum value of these values is re-assigned to the pixel. So the value of each pixel in output image is equal to the minimum value of its neighbors in input image.

Erosion operation is illustrated below using an input image as shown in fig 2.2 where each pixel is assigned a binary value 0 or 1 where 0 represents black color and 1 represents white color.

Fig 2.2 Sample input image for erosion operation

Considering the 4 neighbor structuring element, erosion operations results in output image as shown below in fig 2.3

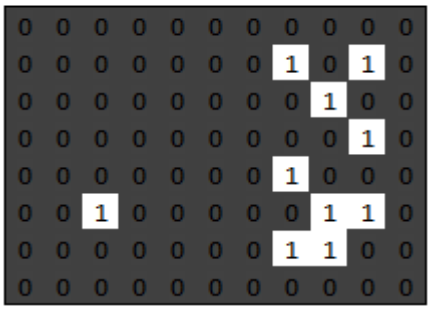


Fig 2.3 Erosion output image

This clearly indicates that the erosion operation erodes the regions boundaries and expands the holes in an input image.

One more example of erosion is shown in below Figure 2.4.

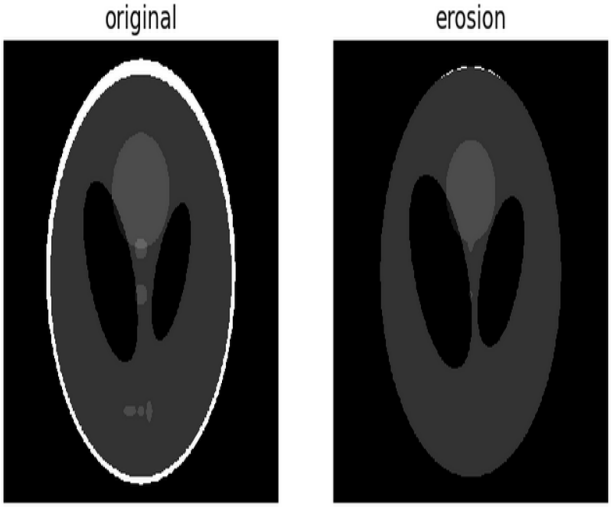


Fig 2.4 Erosion illustration

III. MICROBLAZE PROCESSOR DESIGN

FPGAs are versatile and reusable high-density circuits that can easily be reconfigured by the engineers which allow to quickly perform the VLSI style / validation / simulation cycle at cheaper cost. Various FPGA manufacturers like Xilinx and Altera are encouraged to provide complex embedded parts, as well as multipliers, DSP blocks and even embedded processors due to highly growing need for FPGA device densities. One of the recent subject enhancements in the Xilinx Spartan, Virtex family architectures is the introduction of the Micro Blaze (Soft IP) and PowerPC405 hard-core embedded processor. The MicroBlaze processor is a 32-bit Harvard Reduced Instruction Set pc (RISC) design introduced for implementation in Xilinx FPGAs with separate 32-bit instruction and knowledge buses running at full speed to execute programs and access knowledge from each on-chip and external memory at an equivalent time.

A. Background

The backbone of this design is a single-issue, 3-stage pipeline with thirty two all-purpose registers (without any address registers like the Motorola 68000 Processor), associate in Nursing Arithmetic Logic Unit (ALU), a shift unit, and 2 levels of interrupt. This basic style will then be organized with additional advanced options to tailor to the precise wants of the target embedded application such as: barrel shifter, divider, multiplier, single exactitude on floating-point unit (FPU), instruction and information caches, exception handling, rectify logic, quick Simplex Link (FSL) interfaces at all This flexibility permits the user to balance the specified performance of the target application against the logic space value of the soft processor MicroBlaze additionally supports reset, interrupt, user exception, and break hardware exceptions. For interrupts, MicroBlaze supports only 1 external interrupt supply (connecting to the Interrupt input port). If multiple interrupts are required, then Associate in Nursing interrupt controller should be accustomed handle multiple interrupt requests to MicroBlazeshowninfigure3.1. An interrupt controller is offered to be used with the Xilinx Embedded Development Kit (EDK) code tools. The processor can solely react to interrupts if the Interrupt alter (IE) bit within the Machine standing Register (MSR) is ready to one. On Associate in Nursing interrupt the instruction within the execution stage can complete, whereas the instruction within the decipher stage is replaced by a branch to the interrupt vector (address Ox 10). The interrupt address (the laptop related to the instruction within the decipher stage at the time of the interrupt) is mechanically loaded into all-purpose register. Additionally, the processor additionally disables future interrupts by clearing the id est bit within the MSR. The id est bit is mechanically set once more once corporal punishment the RTlD instruction.

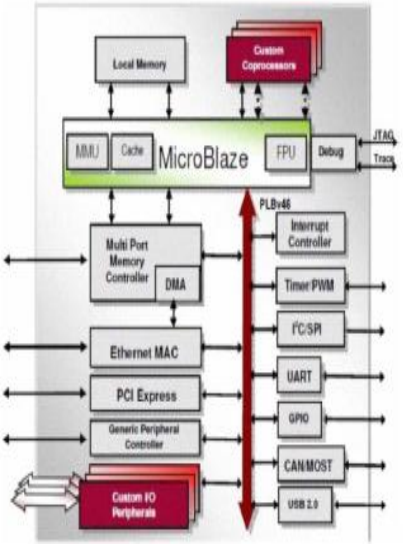


Figure 3.1 MicroBlaze architecture block diagram

Due to the advancement within the fabrication technology and therefore the increase within the density of logic blocks on FPGA, the utilization of FPGA is no longer restricted to debugging and prototyping digital electronic circuits. As a result of the big similarity doable on FPGA and therefore the increasing density of logic blocks, it's getting used currently as a replacement to ASIC solutions during a few applications wherever the time to plug is vital and conjointly entire embedded processor systems square measure enforced on these devices with soft core processors embedded within the system. Soft cores square measure technology freelance and need solely simulation and temporal order verification when synthesized to a target technology. This reduces {style|theplanning|the look} cycle development time by a significance tissue as compared to the event cycle for a tough core processor and has the advantage of customizing the soft core design for a selected application.

B. Features

The Micro Blaze soft core processor is very configurable, permitting you to pick a particular set of options needed by your style.

The fastened feature set of the processor includes:

- Cardinal 32-bit general purpose registers
- 32-bit instruction word with 3 operands and 2 addressing modes
- 32-bitaddressbus
- Single issue pipeline

In addition to those fastened options, the MicroBlaze processor is parameterized to permit selective sanctioning of The Xilinx Platform Studio (XPS) is that the development atmosphere or user interface used for planning the hardware portion of your embedded processor system. B. Embedded Development Kit Xilinx Embedded Development Kit (EDK) is associate integrated software system tool suite for developing embedded systems with Xilinx MicroBlaze and PowerPC CPUs. EDK includes a spread of tools associated applications to help the designer to develop associate embedded system right from the hardware creation to final implementation of the system on an FPGA. System style consists of the creation of the hardware and software system parts of the embedded processor system and also the creation of a verification element is elective. A typical embedded system project requires creation of hardware platform, verification or simulation of hardware platform, creation of software system platform & application, and verification of software system. Base System Builder is the tool to mechanically generate a hardware platform which will satisfy the user specifications defined by the Microprocessor Hardware Specification (MHS) file. [The MHS file defines the system design, peripherals and embedded processors]. The Platform Generation tool creates the hardware platform mistreatment the MHS file as input. The software system platform is defined by MSS (Microprocessor software system Specification) file that defines driver and library customization parameters for peripherals, processor customization parameters, customary one hundred ten devices, interrupt handler routines, and different software systems connected routines. The MSS file is associate input to the Library Generator tool for personalization of drivers, libraries and interrupts handlers.

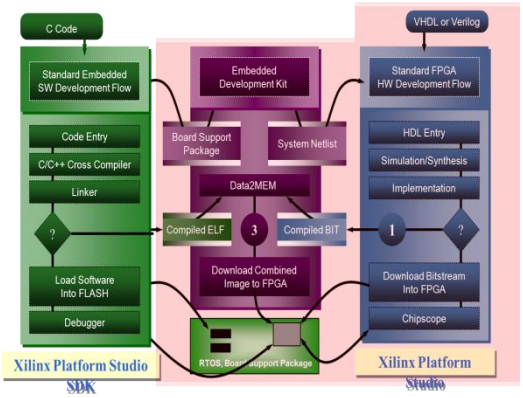
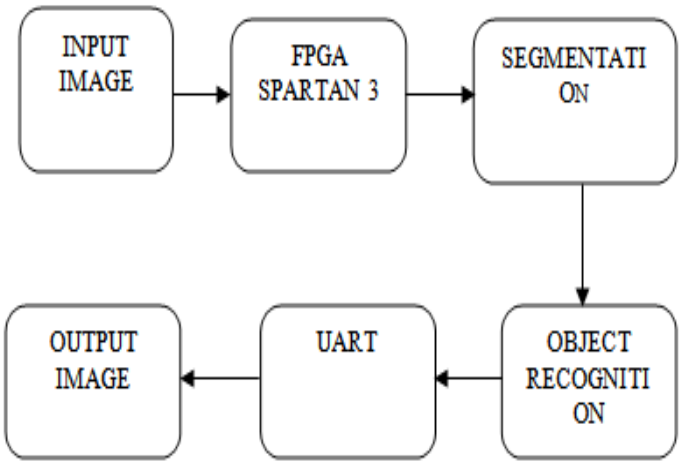


Figure 3.2: Embedded Development Kit Design Flow

The creation of the verification platform is facultative and is predicated on the hardware platform. The MHS file is taken as Associate in Nursing input by the Simgen tool to make simulation files for a particular machine. Three varieties of simulation models will be generated by the Simgen tool: behavioral, structural and temporal arrangement models. Other useful tools on the market in EDK are Platform Studio that provides the GUI for making the MHS and MSS files. Produce / Import IP Wizard that permits the creation of the designer's own peripheral and imports them into EDK. Platform Generator customizes and generates the processor system within the sort of hardware net lists. Library Generator tool configures libraries, device drivers, file systems and interrupt handlers for embedded processor system. Bit stream Initializer tool initializes the instruction memory of processors on the FPGA shown in figure 3.2. Antelope Compiler tools are used for collection and linking application executables for every processor within the system [6]. There are 2 choices on the market for debugging the appliance created victimization EDK namely: Xilinx micro chip correct (XMD) for debugging the appliance package employing a micro chip correct Module (MDM) within the embedded processor system, and package program that invokes the package program appreciate the compiler getting used for the processor. C. package Development Kit Xilinx Platform Studio package Development Kit (SDK) is Associate in Nursing integrated development atmosphere, complimentary to XPS, that's used for C/C++ embedded package application creation and verification. SDK is made on the Eclipse open source framework. Soft Development Kit (SDK) may be a suite of tools that allows you to style a package application for elite Soft IP Cores within the Xilinx Embedded Development Kit (EDK).The package application will be written during a "C or C++" then the entire embedded processor system for user application are completed, else correct and download the bit file into FPGA which acts like a processor.

IV. BLOCK DIAGRAM



object motion detection on background subtraction algorithmic rule. The results obtained by this solution are compared against the traditional software solutions and found more accurate, faster and cost-effective. This system is based on a period pipelined flow on the Micro Blaze architecture of Spartan3 EDK which improves accuracy. The use of pure logic components of FPGA requires low space consumption which makes this approach more cost effective.

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